library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

entity shift\_reg is

port(reset,mode,SerialIN,load: in std\_logic;

Din: in std\_logic\_vector(3 downto 0) ;

Dout: out std\_logic\_vector(3 downto 0));

end shift\_reg;

architecture Shift of shift\_reg is

signal clk: std\_logic:='0';

signal state: std\_logic\_vector(3 downto 0);

begin

tact: process

begin

clk<=not clk;

wait for 50 ns;

end process;

process(clk,reset,mode,load)

begin

if reset='1' then

state<="0000";

elsif clk='1' and clk'event then

if load = '1' then

state<=Din;

elsif mode = '0' then --shift left

state(3 downto 1)<= state(2 downto 0);

state(0)<=SerialIN;

elsif mode='1' then -- shift right

state(3)<=SerialIN;

state(2 downto 0)<=state(3 downto 1);

end if;

end if;

end process;

Dout<=state;

end SHift;

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

entity TB is

end TB;

architecture shift1 of TB is

component shift\_reg is

port(reset,mode,SerialIN,load: in std\_logic;

Din: in std\_logic\_vector(3 downto 0) ;

Dout: out std\_logic\_vector(3 downto 0));

end component;

signal reset,mode,serialIN,load: std\_logic;

signal Din, Dout: std\_logic\_vector(3 downto 0);

begin

ust: Shift\_reg port map(reset,mode,serialIn,load,Din,Dout);

Din<="1101";

process

begin

reset<='1';

mode<='0';

serialIn<='1';

load<='1';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='0';

load<='1';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='0';

load<='1';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='0';

load<='0';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='0';

load<='0';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='1';

load<='0';

wait for 50 ns;

reset<='0';

mode<='0';

serialIn<='1';

load<='0';

wait for 50 ns;

reset<='0';

mode<='1';

serialIn<='0';

load<='0';

wait for 50 ns;

reset<='0';

mode<='1';

serialIn<='0';

load<='0';

wait for 50 ns;

reset<='0';

mode<='1';

serialIn<='1';

load<='0';

wait for 50 ns;

reset<='0';

mode<='1';

serialIn<='1';

load<='0';

wait for 50 ns;

end process;

end shift1;